What is claimed is:

1. A liquid crystal display, comprising:

a power device;

a display unit array;

a scan driver, coupled to the power device, outputting a plurality of scan signals to the display unit array, wherein the scan driver sequentially outputs the scan signals to the display unit array in normal operation of the liquid crystal display, and the scan driver outputs an erase signal and all the scan signals during shutdown and power on processes of the liquid crystal display;

a selection device having a first input terminal coupled to the power device, a first output terminal coupled to the scan driver, a second output terminal, and a first control terminal, wherein when the first control terminal receives the erase signal, and the selection device couples the first input terminal to the second output terminal; and

a current limiting device, coupled between the second output terminal and the scan driver, limiting instantaneous current from the power device when the scan driver simultaneously outputs all the scan signals.

2. The liquid crystal display as claimed in claim 1, wherein the selection device comprises:

a first switch, having a second input terminal coupled to the first input terminal, a second control terminal coupled to the first control terminal, and a third output terminal coupled to the first output terminal, turned on and coupling the first input terminal to the first output terminal in normal operation; and

a second switch, having a third input terminal, a third control terminal coupled to the first terminal, and forth output terminal coupled to the second output terminal, turned on according to the erase signal and coupling the first input terminal to the second output terminal during shutdown and power on processes.

3. The liquid crystal display as claimed in claim 2, wherein the first and second switches are MOS transistors.

4. The liquid crystal display as claimed in claim 3, wherein the erase signal is at a low voltage level.

5. The liquid crystal display as claimed in claim 4, wherein the first switch is an NMOS transistor and the second switch is a PMOS transistor.

6. The liquid crystal display as claimed in claim 3, wherein the erase signal is at a high voltage level.

7. The liquid crystal display as claimed in claim 6, wherein the first switch is an PMOS transistor and the second switch is a PNMOS transistor.

8. The liquid crystal display as claimed in claim 1, wherein the current limiting device is a resistor.